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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,883	03/24/2004	Adam B. Wilson	CYPR-CD03013	6633

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/808,883	WILSON ET AL.
	Examiner	Art Unit
	Quan Tra	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 8 is rejected under 35 U.S.C. 102(e) as being anticipated by Jaussi et al. (USP 6737909).

Jaussi et al. discloses in figure 5 of trimming voltage comprising: receiving an input voltage (reference voltage); performing a constant load current (current going through the variable resistor) and a constant feedback impedance (at the positive terminal of 304) voltage trim process; and outputting a trimmed voltage (at the gate of 510).

3. Claims 8-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Burger, Jr. et al. (USP 6275090).

As to claim 8, Burger, Jr. et al. discloses in figure 1 of trimming voltage comprising: receiving an input voltage (V_{BG}); performing a constant load current (Iref) and a constant feedback impedance (the impedance of current source 101 is constant because Iref is constant) voltage trim process; and outputting a trimmed voltage (VR).

As to claim 9, figure 1 shows that constant load current and constant feedback impedance voltage trimming process comprises selectively adjusting a load resistance (105 and 106)

wherein a substantially constant load current is maintained, selectively adjusting a divider ratio (103, 104) wherein a desired output voltage is generated; and maintaining a substantially constant feedback impedance for each selected load resistance.

As to claim 10, figure 1 shows the step of selectively adjusting the load resistance comprises selectively shunting one or more resistors (105, 106) of a bias current circuit.

As to claim 11, figure 1 shows the step of selectively adjusting the divider ratio comprises selectively coupling an appropriate one of a plurality of nodes of a voltage divider circuit to an output (102).

As to claim 12, figure 1 shows the step of maintaining the substantially constant feedback impedance comprises fixedly coupling a particular node (102) of a voltage divider circuit to an input of an operational amplifier (110).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi (JP 2000-049283).

As to claims 1 and 8, Ikehashi discloses in figure 10 a voltage trimming circuit comprising: an operational amplifier (OP) coupled to an input node (Vbg) a transistor (P1) coupled to the OP; a voltage divider (R1, R1) coupled to the OP, the transistor, and an output (Vref); and a bias current circuit (R2-Rn) coupled to the voltage divider and a second potential.

Thus, figure 10 shows all limitations of the claim except for "the adjustable resistive load in the bias circuit is configurable to maintain a substantial constant load current through the transistor". However, one having ordinary skill in the art would have realized that the current going through Rb is determined by the ratio of Vbg and resistance Rb (I = Vbg/Rb). If current I is constant, the value of resistor Rb must be changed proportional to the value of voltage Vbg. Therefore, it would have been obvious to one having ordinary skill in the art to select the value of Rb to be changed proportional to the value of Vbg in order to have a constant load current.

As to claim 6, the modified Ikehashi's figure 10 shows that substantially constant Ioad current is adapted to reduce instability in the voltage trim circuit (result).

As to claim 7, the modified Ikehashi's figure 10 shows that the substantially constant feedback path is adapted to reduce instability in the voltage trim circuit.

6. Claims 2, 3 and 9-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi (JP 2000-049283) in view of Wu et al. (USP 6542026).

As to claim 2, the modified figure 10 shows all limitations of the claim except for a multiplexer connected between output node and the voltage divider (Ra, R1). However, Wu et al.'s figure 4 shows a voltage generator having multiplexer (5 bits adjustment) that coupled between voltage divider and output node in order to have an adjustable output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add a multiplexer coupled between Ikehashi's voltage divider and the output for the purpose of providing an adjustable output voltage. Thus, the modified figure 10 shows that the input node is coupled to an inverting input of the operational amplifier; the output of the operational amplifier is coupled to a gate of the transistor; the first potential is coupled to a source of the transistor; a drain of the

transistor is coupled to a first terminal of the voltage divider (Ra, R1 and the multiplexer); a second terminal of the voltage divider circuit is coupled to a non-inverting input of the operational amplifier; a third terminal of voltage divider circuit is coupled to the output a fourth terminal of the voltage divider circuit is coupled to a first terminal of the bias current circuit, and a second terminal of the bias current circuit is coupled to said second potential.

As to claim 3, figure 10 shows that the voltage divider circuit comprises a series resistor (R1, Ra) circuit coupled between the transistor and said bias current circuit, and a plurality of selector elements (in the multiplexer), wherein each selector element is coupled between a corresponding node of the series resistor circuit and the output.

Claims 10-17 are rejected as because the modified figure 10 has similar structure and functions as claimed circuit.

7. Claims 4, 5 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikehashi (JP 2000-049283) in view of Burger, Jr. et al. (USP 6275090).

As to claims 4, Ikehashi's figure 10 fails to show "each shunt element is coupled in parallel with a corresponding one of a first portion of resistors of the series resistor circuit". However, Burger, Jr. et al. figure 1 shows a variable resistor having plurality shunt elements respectively coupled in parallel with a corresponding one of a first portion of resistors. Therefore, it would have been obvious to one having ordinary skill in the art to use Burger et al.'s variable resistor for Ikehashi's variable resistors (R2-Rn) due to doctrine equivalent function.

As to claim 5, the modified Ikehashi's figure 10 further shows that first portion of the

series resistor circuit comprises: a first set of binary weighted resistors (Burger et al.'s 103, 104), and a second set of binary weighted resistors (108, 109).

As to claim 18, the modified Ikehashi's figure 10 shows that the bias current circuit comprises: a second plurality of resistors (Burger et al.'s 103-104 or 103-105) coupled in series, and a plurality of shunt elements (switches), wherein each shunt element is coupled in parallel with one of the second plurality of resistors.

As to claim 19, modified Ikehashi's figure 10 shows that the second plurality of resistors comprise a first set of binary weighted resistances (103, 104); and a second set of binary weighted resistances (105, 106).

As to claim 20, , modified Ikehashi's figure 10 shows that bias current circuit further comprises an additional resistor coupled in series with the second plurality of resistors.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

March 31, 2005